In the claims:

1. (Previously presented) A method of forming a set of insulator plugs in an isolation trench in a semiconductor substrate having a device layer, without the use of CMP, comprising the steps of:

depositing a pad insulator layer having a pad thickness over said device layer surface;

etching a set of isolation apertures through said pad insulator and said device layer to an isolation depth;

depositing in a single deposition step an isolation insulator layer in said isolation apertures to a depth sufficient to fill said isolation apertures above said device layer by a first margin that is less than the thickness of said pad insulator and having a sidewall thickness on isolation aperture walls;

etching said isolation insulator layer such that said sidewall thickness of said isolation insulator on said aperture walls is removed; whereby at least some of said isolation insulator remains disposed on a top surface of said pad insulator as a remaining portion of said isolation insulator layer; and remaining isolation plugs of said isolation insulator layer fill said isolation apertures with an isolation plug surface above said device layer surface by a second margin; and

etching said pad insulator layer with an etchant that does not attack said isolation insulator layer, whereby said pad insulator and said remaining portion of said isolation insulator layer are removed in the same step and said isolation plugs fill said apertures without CMP.

2. (Currently amended) A method according to claim 1, in which said semiconductor substrate ~~wafer~~ is an SOI wafer in which said device layer is formed above a buried insulator layer.

3. (Currently amended) A method according to claim 1, in which said semiconductor substrate ~~wafer~~ is a bulk silicon wafer in which said device layer is formed in said silicon wafer.

4. (Original) A method according to claim 1, in which said pad thickness is such that said sidewall thickness is less than a sidewall threshold amount.

5. (Original) A method according to claim 1, in which said first margin is greater than said sidewall threshold amount.

6. (Original) A method according to claim 2, in which said pad thickness is such that said sidewall thickness is less than a sidewall threshold amount.

7. (Original) A method according to claim 2, in which said first margin is greater than said sidewall threshold amount.

8. (Original) A method according to claim 3, in which said pad thickness is such that said sidewall thickness is less than a sidewall threshold amount.

9. (Original) A method according to claim 3, in which said first margin is greater than said sidewall threshold amount.

10. (Previously presented) A method of forming a set of insulator plugs in an isolation trench in a semiconductor substrate having a device layer, without the use of CMP, comprising the steps of:

depositing a pad insulator layer having a pad thickness;

implanting said pad insulator with ions such that implanted areas of said pad insulator have an etch rate substantially greater than unimplanted areas of said pad insulator;

etching a set of isolation apertures through said device layer to an isolation depth;

depositing in a single deposition step an insulator layer in said isolation apertures to a depth sufficient to fill said isolation apertures above said device layer by a first margin that is less than the thickness of said pad insulator and having a sidewall thickness on isolation aperture walls;

etching said insulator layer such that said sidewall thickness of said insulator on said isolation aperture walls is removed; whereby at least some of said isolation insulator remains disposed on a top surface of said pad insulator as a remaining portion of said isolation insulator layer; and remaining insulator plugs of said insulator layer fill said isolation apertures above said device layer;

and etching said pad insulator layer with an etchant that does not attack said insulator layer, whereby said pad insulator and said remaining portion of said isolation insulator layer are removed and said isolation plugs fill said isolation apertures without CMP.

11. (Original) A method according to claim 10, in which at least areas of pad nitride disposed between apertures separated by greater than a minimum active area distance are implanted.

12. (Original) A method according to claim 10, in which only areas of pad nitride disposed between apertures separated by greater than a minimum active area distance are implanted.

13. (Original) A method according to claim 10, in which said ions have an implantation energy such that less than a threshold amount of ions penetrate said device layer.

14. (Original) A method according to claim 10, in which said ions have an implantation energy such that at least a threshold concentration of ions extend throughout said pad insulator layer.

15. (Original) A method according to claim 10, in which said pad thickness is such that said sidewall thickness is less than a sidewall threshold amount.

16. (Original) A method according to claim 10, in which said first margin is greater than said sidewall threshold amount.

17. (Original) A method according to claim 12, in which said pad thickness is such that said sidewall thickness is less than a sidewall threshold amount.

18. (Original) A method according to claim 12, in which said first margin is greater than said sidewall threshold amount.

19. (Previously presented) A method of forming a set of isolation plugs in an isolation trench in a semiconductor substrate having a device layer without the use of CMP comprising the steps of:

depositing a pad insulator layer having a pad thickness;

etching a set of isolation apertures through said device layer to an isolation depth;

depositing an isolation insulator layer in said isolation apertures to a depth sufficient to fill said isolation apertures above said device layer by a first margin and having a sidewall thickness on isolation aperture walls;

etching said isolation insulator layer such that said sidewall thickness of said isolation insulator on said isolation aperture walls is removed and remaining isolation plugs of said isolation insulator layer fill said apertures substantially coplanar with said device layer, without CMP;

forming a set of field apertures in areas of pad insulator disposed between isolation apertures separated by a minimum active area distance; and

etching said pad insulator layer with an etchant that does not attack said isolation insulator layer, whereby said pad insulator is removed and said isolation plugs fill said aperture without CMP.

20. (Previously presented) A method according to claim 10, in which said implanted areas are formed only in areas of pad nitride disposed between isolation apertures separated by greater than a minimum active area distance.

21. (Previously presented) A method of forming a set of insulator plugs in an isolation trench in a semiconductor substrate having a device layer comprising the steps of:

depositing a pad insulator layer having a pad thickness;

implanting said pad insulator with ions such that implanted areas of said pad insulator have an etch rate substantially greater than unimplanted areas of said pad insulator;

etching a set of isolation apertures through said device layer to an isolation depth;

depositing an insulator layer in said isolation apertures to a depth sufficient to fill said isolation apertures above said device layer by a first margin and having a sidewall thickness on isolation aperture walls;

etching said insulator layer such that said sidewall thickness of said insulator on said isolation aperture walls is removed and remaining insulator plugs of said insulator layer fill said isolation apertures above said device layer;

and etching said pad insulator layer with an etchant that does not attack said insulator layer, whereby said pad insulator is removed and said isolation plugs fill said aperture without CMP, in which said implanted areas are formed only in areas of pad nitride disposed between isolation apertures separated by greater than a minimum active area distance in which said step of etching said insulator layer such that said sidewall thickness of said insulator on said aperture walls is removed and remaining isolation plugs of said insulator layer fill said apertures substantially coplanar with said device layer is performed before said step of forming a set of apertures in areas of pad insulator disposed between isolation apertures separated by a minimum active area distance.

22. (Currently amended) A method according to claim 19 ~~20~~, in which said step of etching said isolation insulator layer such that said sidewall thickness of said isolation insulator on said isolation aperture walls is removed and remaining isolation plugs of said insulator layer fill said apertures substantially coplanar with said device layer is performed after said step of forming a set of field apertures in areas of pad insulator disposed between isolation apertures separated by a minimum active area distance.